Embedded Transmission Line MMIC 1-W Flip Chip Assembly Using a Z-Axis Interconnect

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***Abstract*—This letter describes a new type of electronic packaging topology using embedded transmission-line (ETL) monolithic microwave integrated circuits (MMIC's) along with a new state-of-the-art Z-axis material that acts as a chip adhesive as well as an electrical connection with a carrier substrate. The results from the first two flip chip assemblies that were produced under the Microwave Analog Front End Technology (MAFET) Thrust 2 Program are presented. The flip chip packages provided greater than 1-W package output power on a Kovar housing floor with greater than 8-dB package large signal gain at 11.5 GHz.**

***Index Terms*—Embedded transmission line, flip chip, interconnect, microwave integrated circuits, power FET amplifier.**

I. Introduction

EMBEDDED transmission line flip chip packages offer a host of benefits such as low interconnect and field-effect transistor (FET) source inductance as well as low thermal impedance from the active device to its heat sink. Low interconnect inductances enable high-frequency connections from the chip to the package and from the package to the intended host board. Direct metal connections from the active FET area surface to a high thermal conductivity carrier greatly reduce the thermal impedance of gallium arsenide (GaAs) power amplifiers compared to FET's on 100-μm-thick GaAs substrates. This reduction improves reliability and electrical performance.

The multilayer packaging approach presented in this letter is based on the use of ETL MMIC's combined with a novel Z-axis material that is flip chip-mounted on a microwave package or carrier. The ETL MMIC structure, first described in [1], differs from standard MMIC's in that the GaAs substrate is not thinned (635 μm) and acts primarily as a cover to protect the ETL MMIC. Polyimide layers are patterned with metal lines and filled gold vias ending with a ground plane and signal pads. The electrically thick GaAs substrate typically would cause moding at X-band and higher frequencies if the ground plane were placed on the GaAs surface opposite the active device. In ETL MMIC's, the risk of moding is reduced by placing the ground plane above the active devices on an electrically thin (25-μm-thick) polyimide interconnect layer. To date, ETL MMIC structures have been fabricated that work up to 50 GHz, which is the limitation of the radio frequency (RF) probe station. More work is necessary to study the frequency limitations of this unique topology.

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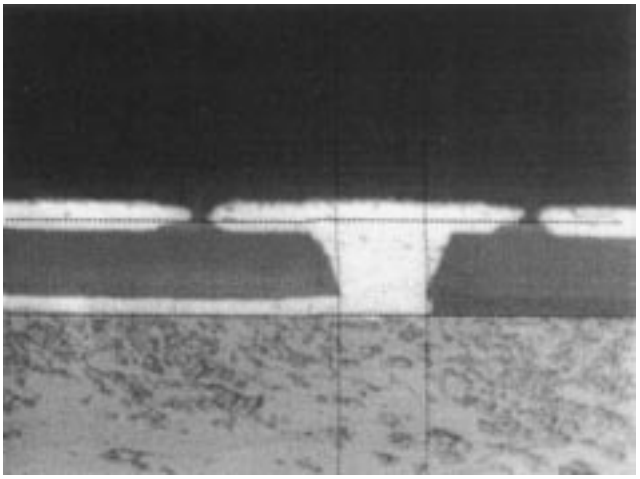

Fig. 1. Cross section of an ETL MMIC interconnect pad. GaAs substrate is shown at the bottom of the photo with air at the top and polyimide between the upper ground plane and the transmission line on the GaAs surface.

II. ETL MMIC's

Fig. 1 displays a cross section of an ETL MMIC interconnect. An inverted microstrip transmission line is shown at the center left as it connects to a solid-plated gold via through a polyimide layer to a pad at the same level as the ground plane. The 25-μm-long via provides an extremely low inductance for the signal line to the outside package. The ETL pHEMT structure is displayed in Fig. 2. The solid-plated metal source plug above the FET region offers extremely low source inductance as well as a low thermal impedance. A 6-μm-high dielectric bridge also serves to reduce the parasitic capacitances introduced by the polyimide.

Fig. 3 displays a photograph of the top side of a 1-W single-stage ETL MMIC amplifier used in the flip chip demonstration along with the layout of the amplifier displayed in Fig. 3. The chip size is 3.03 mm $\times$ 0.96 mm with a 2400-μm ETL pHEMT. The design of this amplifier is accomplished by using an ETL MMIC design library developed under the MAFET Thrust 2 program.

One important consideration during the development of flip chip MMIC's is the ability to perform on-wafer RF probe measurements before and after mounting as well as provide

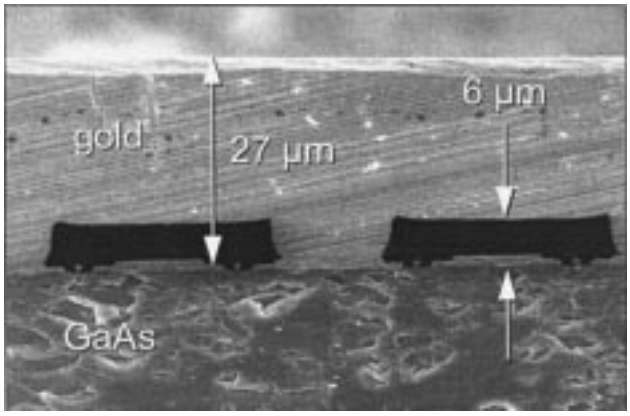

Fig. 2. ETL pHEMT cross section. Four gates are shown with two drain lines and a solid gold-plated source. A 6-μm layer of polyimide encapsulates the FET region.

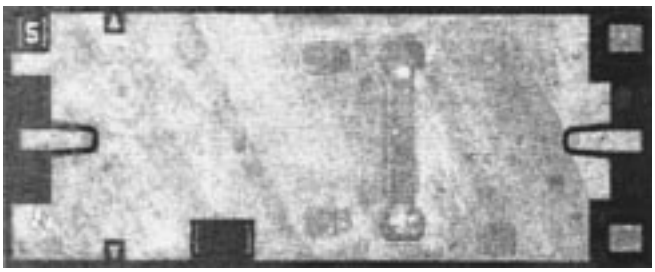

Fig. 3. Photograph of a 1-W single-stage ETL amplifier.

a useful interface to the carrier. For this reason, a tabbed interface was chosen for this particular ETL MMIC. The alignment tolerance of the tabs is the length that the tab extends beyond the ground plane provided that there is no lateral bridging of the interconnect material (e.g., solder, silver epoxy, z-axis material, etc., ...).

ETL MMIC's have a significant advantage compared to other MMIC packaging configurations: their S-parameters change very little when the chip is mounted or encapsulated because the MMIC is already shielded with a ground plane. As with all packaging schemes, interconnect inductances and transitions should be defined early and taken into account during the design process to avoid unnecessary surprises later in the system design cycle.

The ETL pHEMT models used for the EG9907 are based on measurements and models of conventional pHEMT's on 100-μm GaAs whose parasitic capacitances have been increased based on electrostatic two-dimensional (2-D) simulations to account for the effects of polyimide encapsulation. Measurements from ETL wafers have demonstrated greater than 9-dB small signal gain at 12 GHz with a drain bias of 5 V and a source-drain current of 180 mA. Fig. 4 displays S_{21} of 20 single-stage amplifiers from a single wafer.

III. Z-Axis Material

The Z-axis material used in this assembly consists of a host dielectric that has been perforated with micrometer-sized holes. Gold wires are formed through a plating operation. The material is cut into a preform and is placed between the carrier

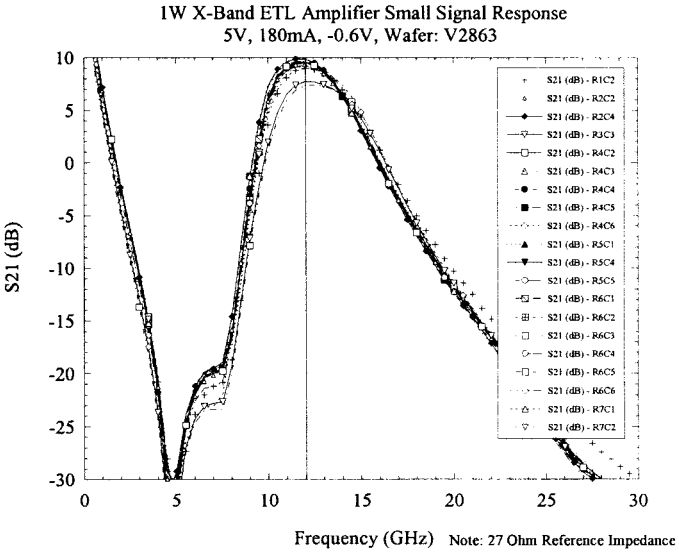

Fig. 4. Small-signal S_{21} of a 1-W X-band ETL amplifier from wafer V2863. Average MMIC response demonstrates more than 9 dB of gain at 12 GHz.

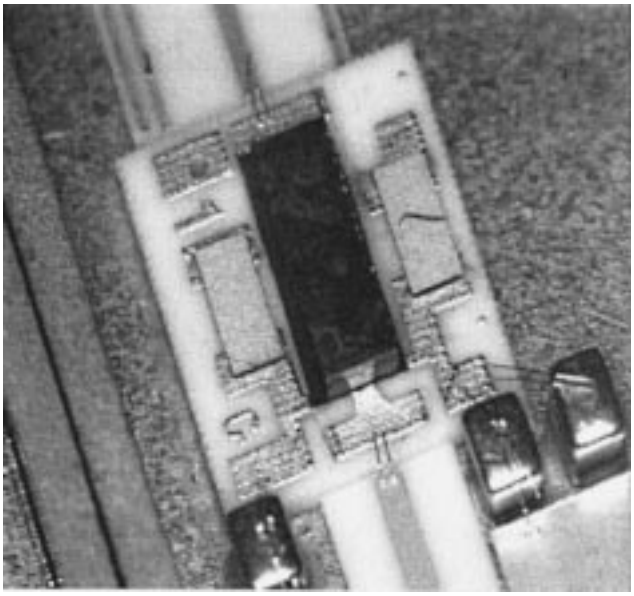

Fig. 5. ETL MMIC flip chip assembly showing an ETL MMIC (center) with two flip chip capacitors on each side of the MMIC on a 20-ml-thick BeO carrier.

and the MMIC. Pressure and temperature on the MMIC and carrier make the host dielectric adhere mechanically to the chip and carrier while the microwires press and complete the electrical connections.

IV. Flip Chip Package

The ETL MMIC flip chip package that has been mounted inside the module is displayed in Fig. 5. The ETL MMIC is seen in the center mounted on a 500-μm-thick BeO ceramic thick film carrier. Grounding to the ETL MMIC is accomplished using filled through vias. Two 100-pF capacitors from Dielectric Labs are mounted on either side of the ETL MMIC using silver epoxy. Z-axis material is used to mount the ETL MMIC to the BeO carrier and is visible as a thin black sheet

to the left of the ETL MMIC. The reflection of the output transmission line can be seen on the lower outside GaAs face of the ETL MMIC. Gate and drain biases are supplied on either side of the BeO chip with 0.01-μF capacitors end mounted with silver epoxy to the module floor. Input and output transmission lines are 50-Ω microstrip lines on alumina.

The flip chip assembly was mounted within a module and tested within a connectorized test fixture. Uncorrected peak output power of 29.4 dBm is measured for this assembly at 11.5 GHz (including test fixture losses). The power-added efficiency was measured to be 26.6%. The results include losses due to input and output connectors, alumina microstrip lines, module feed throughs, and wirebonds. The total loss of a passive through line in the test fixture is measured to be 2.1 dB at 11.5 GHz with 0.7 dB estimated for the output passive network loss and 1.4 dB for the input passive network loss.

V. Conclusions

The flip chip assembly presented in this work demonstrates the advantages of the ETL MMIC approach combined with Z-axis material for package insertion into a conventional module. The low inductance interconnects reduce the complexity of design at X band because bondwire inductance and variability did not need to be taken into account. By operating in the flip chip configuration, the surface density of active components compared with the unused areas can be significantly increased. ETL MMIC's are capable of millimeter-wavelength operation [1] and offer promising performance for future high-frequency low-noise and power amplifier applications.

Acknowledgment

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References

[1] H. Tserng, P. Saunier, A. Ketterson, L. Witkowski, and T. Jones, "Embedded transmission line (ETL) MMIC for low-cost, high-density wireless communication applications," in *IEEE Radio Freq. Integrated Circuits Symp.*, 1997, pp. 41–44.